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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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FOLEY & LARDNER 150 EAST GILMAN STREET P.O. BOX 1497 MADISON, WI 53701-1497			EXAMINER DICKEY, THOMAS L	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 09/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/772,573

Applicant(s)

MAWST ET AL. 

Examiner

Thomas L. Dickey

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 June 2005.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-65 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-21, 23-29, 32, 34-46, 48-56, 59 and 62-65 is/are rejected.
7) ☒ Claim(s) 22, 30, 31, 33, 47, 57, 60 and 61 is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 05 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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DETAILED ACTION

1. The amendment filed on 6/29/05 has been entered.
2. New art has been applied to some of Applicant's claims. Consequently this action is Non-Final.

Priority

3. Applicants have made no claim for priority.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

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A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1,2,8,11,12,15, 16,17,18-21,23,24,25,26, 27,29,32,34,38, 39,48,49,52,53, 54,58, 59, 62, and 63 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-33 of U.S. Patent No. 6,791,104 in view of PETER ET AL. ("Light-emitting diodes and laser diodes based on a $\text{Ga}_{1-x}\text{In}_x\text{As}/\text{GaAs}_{1-y}\text{Sb}_y$ " Applied Physics Letters, 04/05/99, Vol. 74 Issue 14, pp1951-1953).

With regard to claims 1,2,8,11,12,15,53, and 54, claims 1-33 of Patent No. 6,791,104 disclose an optoelectronic device comprising a multilayer semiconductor structure including a substrate and an active region, the active region comprising at least a hole quantum well layer of a semiconductor containing antimony and at least one electron quantum well layer adjacent to the hole quantum well layer which comprises a semiconductor containing nitrogen to provide a type II quantum well

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structure, wherein the semiconductor containing antimony is InGaAsSb and the semiconductor containing nitrogen is InAsN, wherein the semiconductor containing antimony is GaAsSb or InGaAsSb and the semiconductor containing nitrogen is InAsN or InGaAsN, wherein the electron quantum well layers and hole quantum well layer form a first quantum well stage, and wherein the active region comprises a plurality of quantum well stages adjacent to each other each having electron quantum well layers surrounding a hole quantum well layer, including means for providing optical feedback to form an edge-emitting laser or a vertical cavity surface-emitting laser.

Claims 1-33 do not disclose that the substrate is an InP substrate. However, Peter et al. discloses an optoelectronic device with an InP substrate. Note the first column of page 1951 of Peter et al. Peter et al. explain that the binary InP substrate is advantageous in that it is commercially used and thus technically advanced, has good thermal conductivity and low electrical resistance. Therefore, it would have been obvious to a person having skill in the art to replace the substrate of the device of claims 1-33 with the InP substrate such as taught by Peter et al. in order to provide a substrate that is technically advanced, has good thermal conductivity and low electrical resistance to thus provide higher reliability.

With regard to claims 16,17,18-21,23,24,25,26, and 59, claims 1-33 of Patent No. 6,791,104 disclose an optoelectronic device comprising a multilayer semiconductor

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structure including a substrate and an active region, the active region comprising at least a hole quantum well layer of GaAsSb or InGaAsSb and an electron quantum well layer of InAsN or InGaAsN on each side of the hole quantum well layer to provide a type II quantum well structure, wherein the electron quantum well layers are in compressive strain and the hole quantum well layer is in compressive strain and the thickness of each electron quantum well layer and hole quantum well layer is between approximately 10 and 50 angstroms, wherein the electron quantum well layers and hole quantum well layer form a first quantum well stage, and wherein the active region comprises a plurality of quantum well stages adjacent to each other and the electron quantum well layer is an InAsN layer, wherein the hole quantum well layer is an InGaAsSb layer and the electron quantum well layer is an InAsN layer, and including means for providing optical feedback to form an edge-emitting laser or a vertical cavity surface-emitting laser.

Claims 1-33 do not disclose that the substrate is an InP substrate. However, Peter et al. discloses an optoelectronic device with an InP substrate. Note the first column of page 1951 of Peter et al. Peter et al. explain that the binary InP substrate is advantageous in that it is commercially used and thus technically advanced, has good thermal conductivity and low electrical resistance. Therefore, it would have been obvious to a person having skill in the art to replace the substrate of the device of claims

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1-33 with the InP substrate such as taught by Peter et al. in order to provide a substrate that is technically advanced, has good thermal conductivity and low electrical resistance to thus provide higher reliability.

With regard to claims 27,29,32,34, and 38, claims 1-33 of Patent No. 6,791,104 disclose an optoelectronic device comprising a multilayer semiconductor structure including a substrate and an active region, the active region comprising at least a hole quantum well layer of GaAsSb and an electron quantum well layer of InAsN on each side of the hole quantum well layer to provide a type II quantum well structure wherein the electron quantum well layers are in compressive strain and the hole quantum well layer is in compressive strain, wherein the thickness of each electron quantum well layer and hole quantum well layer is between approximately 10 and 50 angstroms, wherein the electron quantum well layers and hole quantum well layer form a first quantum well stage, and wherein the active region comprises a plurality of quantum well stages adjacent to each other, and including means for providing optical feedback to form an edge-emitting laser or a vertical cavity surface-emitting laser.

Claims 1-33 do not disclose that the substrate is an InP substrate. However, Peter et al. discloses an optoelectronic device with an InP substrate. Note the first column of page 1951 of Peter et al. Peter et al. explain that the binary InP substrate is advantageous in that it is commercially used and thus technically advanced, has good

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thermal conductivity and low electrical resistance. Therefore, it would have been obvious to a person having skill in the art to replace the substrate of the device of claims 1-33 with the InP substrate such as taught by Peter et al. in order to provide a substrate that is technically advanced, has good thermal conductivity and low electrical resistance to thus provide higher reliability.

With regard to claims 39,48,49,52,62 and 63, claims 1-33 of Patent No. 6,791,104 disclose an semiconductor laser comprising (a) a multilayer semiconductor structure including a substrate and an active region, the active region comprising at least a hole quantum well layer of a semiconductor containing antimony and at least one electron quantum well layer comprising a semiconductor containing nitrogen adjacent to the hole quantum well layer to provide a type II quantum well structure; and (b) means for providing optical feedback to provide lasing action in the active region, wherein the means for providing optical feedback forms an edge-emitting laser or a vertical cavity surface-emitting laser, wherein the semiconductor containing antimony is InGaAsSb the semiconductor containing nitrogen is InAsN.

Claims 1-33 do not disclose that the substrate is an InP substrate. However, Peter et al. discloses an optoelectronic device with an InP substrate. Note the first column of page 1951 of Peter et al. Peter et al. explain that the binary InP substrate is advantageous in that it is commercially used and thus technically advanced, has good

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thermal conductivity and low electrical resistance. Therefore, it would have been obvious to a person having skill in the art to replace the substrate of the device of claims 1-33 with the InP substrate such as taught by Peter et al. in order to provide a substrate that is technically advanced, has good thermal conductivity and low electrical resistance to thus provide higher reliability.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,2,8,11-18,21,24,25,26,27,28,29,32,34-46,48-51,54,59, and 63-65 are rejected under 35 U.S.C. 102(b) as being anticipated by PETER ET AL. ("Light-emitting diodes and laser diodes based on a $\text{Ga}_{1-x}\text{In}_x\text{As}/\text{GaAs}_{1-y}\text{Sb}_y$ " Applied Physics Letters, 04/05/99, Vol. 74 Issue 14, pp1951-1953).

With regard to claims 1,2,8, 11-14, and 54 Peter et al. disclose a multilayer semiconductor structure including an InP substrate and an active region, the active region comprising at least a hole quantum well layer of a semiconductor containing

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antimony and at least one electron quantum well layer adjacent to the hole quantum well layer which comprises a semiconductor containing nitrogen to provide a type II quantum well structure, wherein the semiconductor containing nitrogen is InAsN, the semiconductor containing antimony is GaAsSb or InGaAsSb and the semiconductor containing nitrogen is InAsN or InGaAsN, the electron quantum well layers and hole quantum well layer form a first quantum well stage, and wherein the active region comprises a plurality of quantum well stages adjacent to each other each having electron quantum well layers surrounding a hole quantum well layer, and the active region generates light having a wavelength greater than approximately 2 microns or approximately 3 microns and including means for providing optical feedback to form an edge-emitting laser or a vertical cavity surface-emitting laser.

With regard to claims 16,17,18,20,21,24,25,26, and 59 Peter et al. disclose a multilayer semiconductor structure including an InP substrate and an active region, the active region comprising at least a hole quantum well layer of GaAsSb or InGaAsSb and an electron quantum well layer of InAsN or InGaAsN on each side of the hole quantum well layer to provide a type II quantum well structure, wherein the electron quantum well layer is an InAsN layer, the electron quantum well layers are in compressive strain and the hole quantum well layer is in compressive strain, the thickness of each electron quantum well layer and hole quantum well layer is between approximately 10 and 50

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angstroms, the electron quantum well layers and hole quantum well layer form a first quantum well stage, and wherein the active region comprises a plurality of quantum well stages adjacent to each other, and including means for providing optical feedback to form an edge-emitting laser or a vertical cavity surface-emitting laser.

With regard to claims 27,28,29,32, and 34-38 Peter et al. disclose a multilayer semiconductor structure including an InP substrate and an active region, the active region comprising at least a hole quantum well layer of GaAsSb and an electron quantum well layer of InAsN on each side of the hole quantum well layer to provide a type II quantum well structure wherein the electron quantum well layers are in compressive strain and the hole quantum well layer is in compressive strain, wherein (at least one of) the electron quantum well layers is lattice matched to InP, the thickness of each electron quantum well layer and hole quantum well layer is between approximately 10 and 50 angstroms, the electron quantum well layers and hole quantum well layer form a first quantum well stage, and wherein the active region comprises a plurality of quantum well stages adjacent to each other, the active region generates light having a wavelength greater than approximately 2 microns or approximately 3 microns, and including means for providing optical feedback to form an edge-emitting laser or a vertical cavity surface-emitting laser.

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With regard to claims 39,40-46,48-51, and 63-65 Peter et al. disclose a semiconductor laser including (a) an InP substrate and an active region, the active region comprising at least a hole quantum well layer of a semiconductor containing antimony and at least one electron quantum well layer comprising a semiconductor containing nitrogen adjacent to the hole quantum well layer to provide a type II quantum well structure; wherein there is an electron quantum well layer on each side of the hole quantum well layer and there is a barrier layer adjacent to each electron quantum well layer on each side of the hole quantum well layer to provide a conduction band profile for the active region having a W-shaped configuration, the semiconductor containing antimony is GaAsSb or InGaAsSb and the semiconductor containing nitrogen is InAsN or InGaAsN, the electron quantum well layers are in compressive strain and the hole quantum well layer is in compressive strain, wherein the electron quantum well layers are in compressive strain and the hole quantum well layer is in tensile strain, the thickness of each electron quantum well layer and hole quantum well layer is between approximately 10 and 50 angstroms, the electron quantum well layers and hole quantum well layer form a first quantum well stage, and wherein the active region comprises a plurality of quantum well stages adjacent to each other each having electron quantum well layers surrounding a hole quantum well layer, the active region generates light having a wavelength greater than approximately 2 microns or 3 microns,

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the semiconductor containing nitrogen is InAsN, and wherein there is an optical confinement layer adjacent to each barrier layer, the optical confinement layer comprising InP, and (b) means for providing optical feedback to provide lasing action in the active region, the means for providing optical feedback forming an edge-emitting laser or a vertical cavity surface-emitting laser..

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-10 and 54-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over DAPKUS (6,621,842) in view of PETER ET AL. ("Light-emitting diodes and laser diodes based on a $Ga_{1-x}In_xAs/GaAs_{1-y}Sb_y$ " Applied Physics Letters, 04/05/99, Vol. 74 Issue 14, pp1951-1953).

With regard to claims 1,2,3-7,54,55, and 56 Dapkus discloses an optoelectronic device comprising a multilayer semiconductor structure including an substrate and an active region, the active region comprising at least a hole quantum well layer of a semiconductor containing antimony and at least one electron quantum well layer

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adjacent to the hole quantum well layer which comprises a semiconductor containing nitrogen to provide a type II quantum well structure, wherein the semiconductor containing antimony is GaAsSb or InGaAsSb, there is an electron quantum well layer on each side of the hole quantum well layer and there is a GaInP barrier layer adjacent to each electron quantum well layer on each side of the hole quantum well layer to provide a conduction band profile for the active region having a W-shaped configuration. Note figures 2-4, column 5 lines 1-67, column 6 lines 1-67, and column 7 lines 1-29 of Dapkus.

Dapkus does not disclose that the substrate is an InP substrate. However, Peter et al. discloses an optoelectronic device with an InP substrate. Note the first column of page 1951 of Peter et al. Peter et al. explain that the binary InP substrate is advantageous in that it is commercially used and thus technically advanced, has good thermal conductivity and low electrical resistance. Therefore, it would have been obvious to a person having skill in the art to replace the substrate of the device of Dapkus with the InP substrate such as taught by Peter et al. in order to provide a substrate that is technically advanced, has good thermal conductivity and low electrical resistance to thus provide higher reliability.

With regard to claims 1,8,9, and 10 Dapkus discloses an optoelectronic device comprising a multilayer semiconductor structure including an substrate and an active

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region, the active region comprising at least a hole quantum well layer of a semiconductor containing antimony and at least one electron quantum well layer adjacent to the hole quantum well layer which comprises a semiconductor containing nitrogen to provide a type II quantum well structure, wherein the electron quantum well layers and hole quantum well layer form a first quantum well stage, and wherein the active region comprises a plurality of quantum well stages adjacent to each other each having electron quantum well layers surrounding a hole quantum well layer, and including a GaInP barrier layer between each quantum well stage to provide a conduction band profile having a W-shaped configuration. Note figures 2-4, column 5 lines 1-67, column 6 lines 1-67, and column 7 lines 1-29 of Dapkus.

Dapkus does not disclose that the substrate is an InP substrate. However, Peter et al. discloses an optoelectronic device with an InP substrate. Note the first column of page 1951 of Peter et al. Peter et al. explain that the binary InP substrate is advantageous in that it is commercially used and thus technically advanced, has good thermal conductivity and low electrical resistance. Therefore, it would have been obvious to a person having skill in the art to replace the substrate of the device of Dapkus with the InP substrate such as taught by Peter et al. in order to provide a substrate that is technically advanced, has good thermal conductivity and low electrical resistance to thus provide higher reliability.

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Allowable Subject Matter

7. Claims 22,30,31,33,47,57,60 and 61 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments with respect to claims 1-52 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

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information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'T. L. Dickey', is positioned above the printed name.

Thomas L. Dickey
Patent Examiner
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08/05